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Box Patent Application Assistant Commissioner for Patents Washington, D.C. 20231

New U.S. Patent Application

Title: METHOD FOR FORMING GATE ELECTRODES IN A SEMICONDUCTOR DEVICE USING FORMED FINE

PATTERNS

inventors: 1) Jun Dong KIM

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ALO ALTO

We enclose the following papers for filing in the United States Patent and Trademark Office in connection with the above patent application.

- 1. Application - 11 pages, including 2 independent claims and 12 claims total.
- 2. Drawings - 4 sheets of formal drawings containing 7 figures.
- 3. Certified copy of Korean Application No. 2000-36495, filed June 29, 2000.
- 4. The filing fee is calculated as follows:

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Basic Application Filing Fee					\$710	\$	710.00
	Number of Claims		Basic	Extra Claims			
Total Claims	12	-	20		x \$18		
Independent Claims	2	-	3		x \$80		
[X] Presentation of Multiple Dep. Claim(s) +\$270							270.00
Subtotal						\$	980.00
Reduction by 1/2 if small entity						-	
TOTAL APPLICATION FILING FEE						\$	980.00

5. A check for \$980.00 is enclosed. The fee includes

\$710.00 filing fee; and \$270.00 Multiple Dependant Claims

This application is being filed under the provisions of 37 C.F.R. § 1.53(f). Applicants await notification from the Patent and Trademark Office of the time set for filing the Declaration.

Applicants claim the right to priority based on Korean Application No. 2000-36495, filed June 29, 2000.

Please address all correspondence with respect to this application to:

Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P. 1300 I Street, N.W. Washington, D.C. 20005-3315

Please accord this application a serial number and filing date.

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The Commissioner is hereby authorized to charge any additional filing fees due and any other fees due under 37 C.F.R. § 1.16 or § 1.17 during the pendency of this application to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Ernest F. Chapman Reg. No. 25,961

EFC/FPD/bl Enclosures